Le87612

PLC Dual Channel Class AB Line Driver
Line Driver BD870 Series

Preliminary Data Sheet

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FEATURES

- 28-pin, 4x5 mm QFN Package
- Very low power dissipation
  - Class AB operation
- 4 programmable states
- No external gain resistors required
- RoHS compliant

APPLICATIONS

- Power Line Communications
- Home Networking
- HPNA
- G.HN

DESCRIPTION

The Le87612 is a dual channel differential amplifier designed to work in Home Plug Alliance HPAV2 systems with very low power dissipation.

The Le87612 contains two pairs of wideband amplifiers designed with Microsemi's HV15 Bipolar SOI process for low power consumption.

The line driver gain is fixed internally. The amplifiers are powered from a single supply.

The device can be programmed to one-of-three preset Bias levels or to a Disable state. Each channel can be controlled independently. The control pins respond to input levels that can be generated with a standard tri-state GPIO.

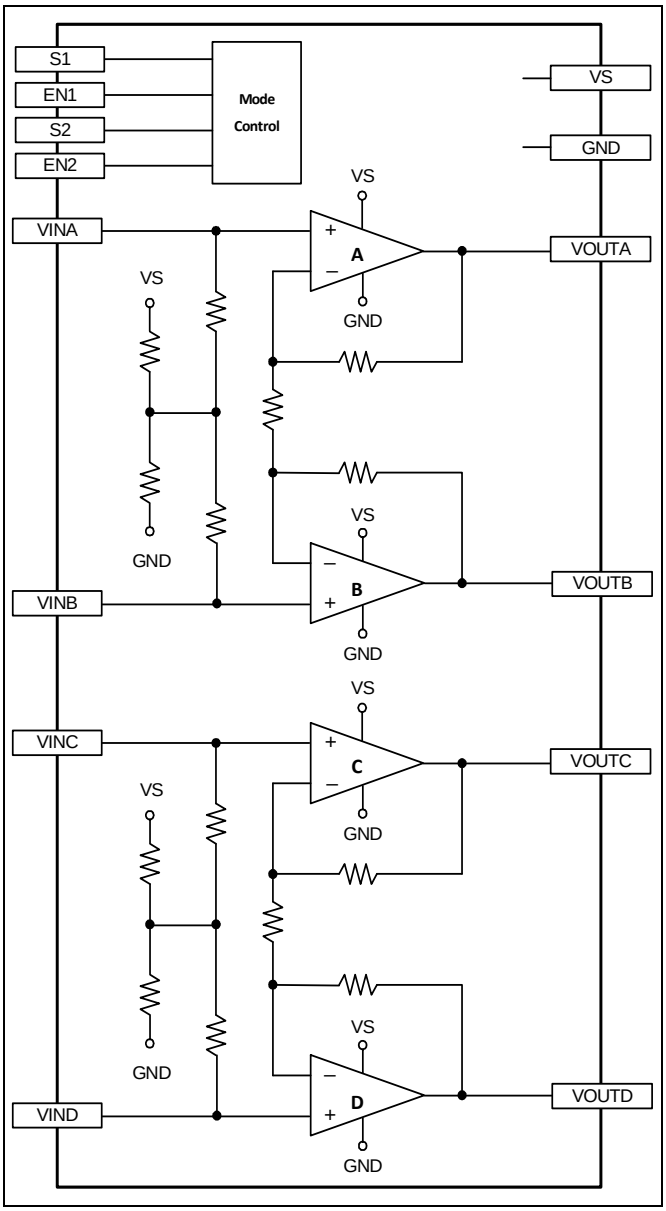
The Le87612 is available in a 28-pin (4 mm x 5 mm) QFN package with exposed pad for enhanced thermal conductivity.

ORDERING INFORMATION

Le87612MQC	28-pin QFN Green Package	Tray
Le87612MQCT	28-pin QFN Green Package	Tape and Reel

The green package meets RoHS 2 Directive 2011/65/EU of the European Council to minimize the environmental impact of electrical equipment.

BLOCK DIAGRAM



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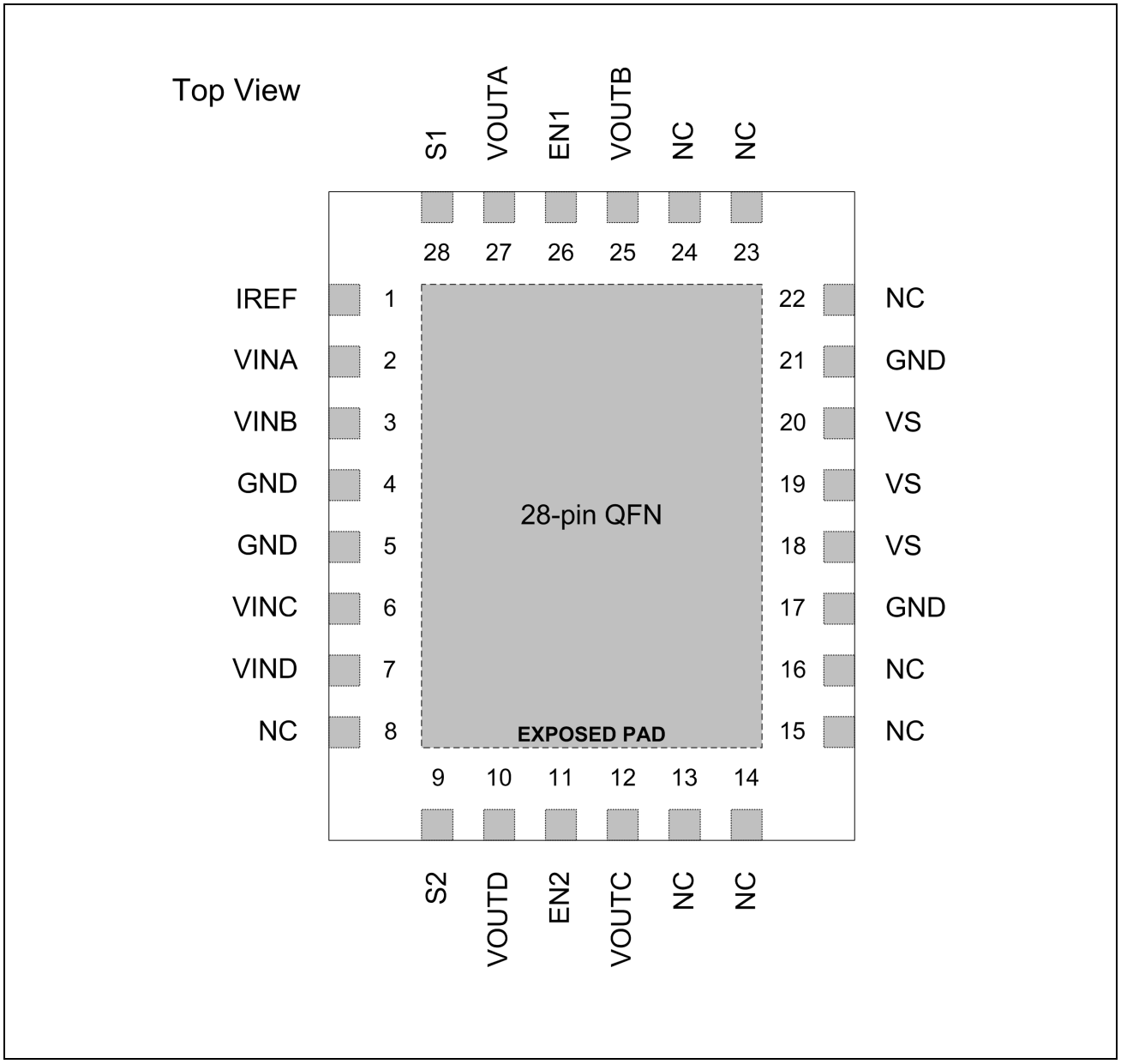
CONNECTION DIAGRAM



Note:

1. *Pin 1 is marked for orientation.*
2. *The Le87612 device incorporates an exposed die pad on the underside of its package. The pad acts as a heat sink and must be connected to a copper plane through thermal vias, for proper heat dissipation. It is electrically isolated and maybe connected to GND.*

PIN DESCRIPTIONS

Pin #	Pin Name	Type	Description
1	IREF	Input	Device internal reference current. Connect a resistor (R_{REF}) to GND.
2	VINA	Input	Non-inverting input of amplifier A
3	VINB	Input	Non-inverting input of amplifier B
4	GND	Ground	Reference ground
5	GND		
6	VINC	Input	Non-inverting input of amplifier C
7	VIND	Input	Non-inverting input of amplifier D
8	NC		No internal connection
9	S2	Input	Channel 2 state control
10	VOUTD	Output	Amplifier D output
11	EN2	Input	Enable Channel 2 transmission
12	VOUTC	Output	Amplifier C output
13	NC		No internal connection
14	NC		
15	NC		
16	NC		
17	GND	Ground	Reference ground
18	VS	Power	Power Supply, +12 V
19	VS		
20	VS		
21	GND	Ground	Reference ground
22	NC		No internal connection
23	NC		
24	NC		
25	VOUTB	Output	Amplifier B output
26	EN1	Input	Enable Channel 1 transmission
27	VOUTA	Output	Amplifier A output
28	S1	Input	Channel 1 state control
	Exposed pad		Electrically isolated thermal conduction pad, can be grounded

ABSOLUTE MAXIMUM RATINGS

Stresses above the values listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage Temperature	$-65 \le T_A \le +150$ °C
Operating Junction Temperature (1)	$-40 \le T_j \le +150$ °C
VS with respect to GND	-0.3 V to +16 V
Control inputs with respect to GND	-0.3 V to 4 V
Continuous Driver Output Current	100 mA
Maximum device power dissipation, continuous (2) - T_A = 85°C, P_D	1.0 W
Junction to ambient thermal resistance (2,3), θ_{JA}	36.0 °C/W
Junction to board thermal resistance (2), θ_{JB}	18.3 °C/W
Junction to case bottom (exposed pad) thermal resistance, $\theta_{JC\ (BOTTOM)}$	8.9 °C/W
Junction-to-top characterization parameter (2), ψ_{JT}	1.2 °C/W
ESD Immunity (Human Body Model)	JESD22 Class 2 compliant
ESD Immunity (Charge Device Model)	JESD22 Class IV compliant

Notes:

1. *Continuous operation above 145°C junction temperature may degrade device reliability.*
2. *See Thermal Resistance.*
3. *No air flow.*

Thermal Resistance

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to larger internal copper planes.

Package Assembly

The green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes.

Refer to IPC/JEDEC J-Std-020 Table 4 for recommended peak soldering temperature and Table 5-2 for the recommended solder reflow temperature profile.

OPERATING RANGES

Microsemi guarantees the performance of this device over the 0°C to 85°C temperature range by conducting electrical characterization over each range and by conducting a production test with single insertion coupled with periodic sampling. These characterization and test procedures comply with the Telcordia GR-357-CORE Generic Requirements for Assuring the Reliability of Components Used in Telecommunications Equipment.

Ambient temperature	T_A	0°C to +85°C
Power Supply	VS with respect to GND	+12 V ± 5%

DEVICE SPECIFICATIONS

Typical Conditions: As shown in the basic test circuit (Figure 1) with VS = +12 V, R_{REF} = 75 kΩ, and T_A = 25°C.

Min/Max Parameters: T_A = 0 to +85°C.

Table 1. Electrical Specifications

Symbol	Parameter Description	Condition	Min	Typ	Max	Unit	Notes
Supply Current Characteristics							
I_{VS}	Supply Current (per channel)	Full Power State	17	23	29	mA	
		Medium Power State	11	19	23		
		Low Power State	5	10.5	15		
		Disable State		1	1.5		
Control Input (S1, S2, EN1, EN2) Specifications							
V_{IH}	Input High Voltage		2.0	3.3	3.6	V	
V_{IM}	Input Middle Voltage (S1, S2)			1.5		V	
V_{IL}	Input Low Voltage		-0.3	0	0.8	V	
	Enable Time			500		ns	
Amplifier Characteristics							
	Differential Gain	Full Power State, VOUT/VIN	8.2	8.7	9.0	V/V	
	Bandwidth, -3 dB	Full Power State		200		MHz	
		Medium Power State		200			
		Low Power State		115			
V_O	Output Voltage			10		V	
I_O	Output Current		150			mA	1
Z_I	Input Impedance	Differential	13	15	18	kΩ	
Amplifier Dynamic Characteristics							
Noise	Input Referred Noise	2 – 106 MHz		9	15	$nV/\sqrt{Hz}$	1
TSD	Thermal Shutdown Temperature			170		°C	

Notes:

1. Not tested in production. Guaranteed by characterization and design.

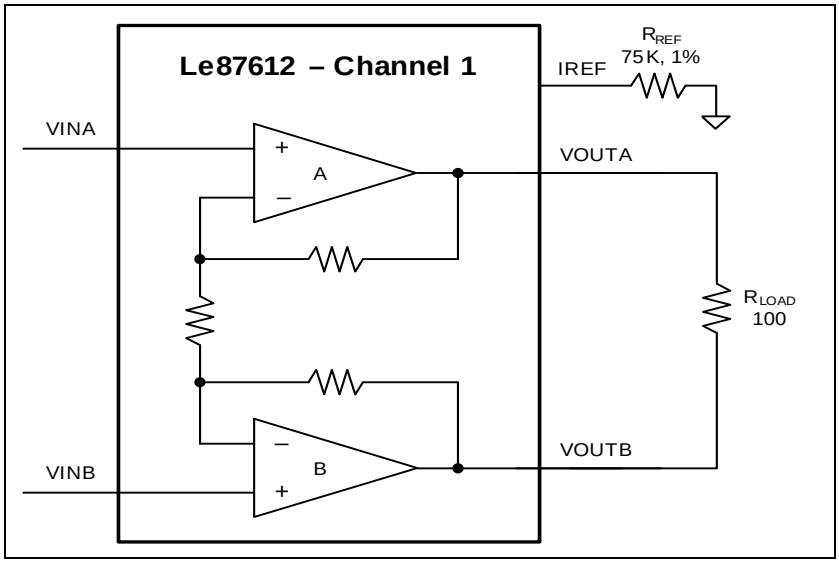


Figure 1. Basic Test Circuit

STATE CONTROL

S1, EN1 and S2, EN2 pins are used as combinatorial logic inputs to control the line driver operating states. Table 3 and Table 3 show the programmable states for each channel.

S1 and S2 are tri-state inputs that accept three operating levels. These pins have internal resistors tied to +1.5 V which force a middle logic input level when the control to these pins is tri-stated.

Table 2. Channel 1 Control Matrix

S1	EN1	State
X	0	Disable
0	1	Enable Low Bias
Open	1	Enable Medium Bias
1	1	Enable Full Bias

Table 3. Channel 2 Control Matrix

S2	EN2	State
X	0	Disable
0	1	Enable Low Bias
Open	1	Enable Medium Bias
1	1	Enable Full Bias

Disable State: Amplifier bias current removed. This is the lowest power state. Amplifier output is high impedance. Gain-setting feedback resistors are still connected across amplifier output pins, creating 1300 ohm differential impedance at pins.

Bias States: Line Driver is active for transmission. States are different only in the amount of bias current to the amplifiers, and therefore power consumption. There is a trade-off between bias current and bandwidth.

APPLICATIONS

The Le87612 integrates two sets of high-power line driver amplifiers designed for low distortion for signals up to 106 MHz.

Figure 2 shows an application circuit of channel 1 with amplifiers A and B in transmission.

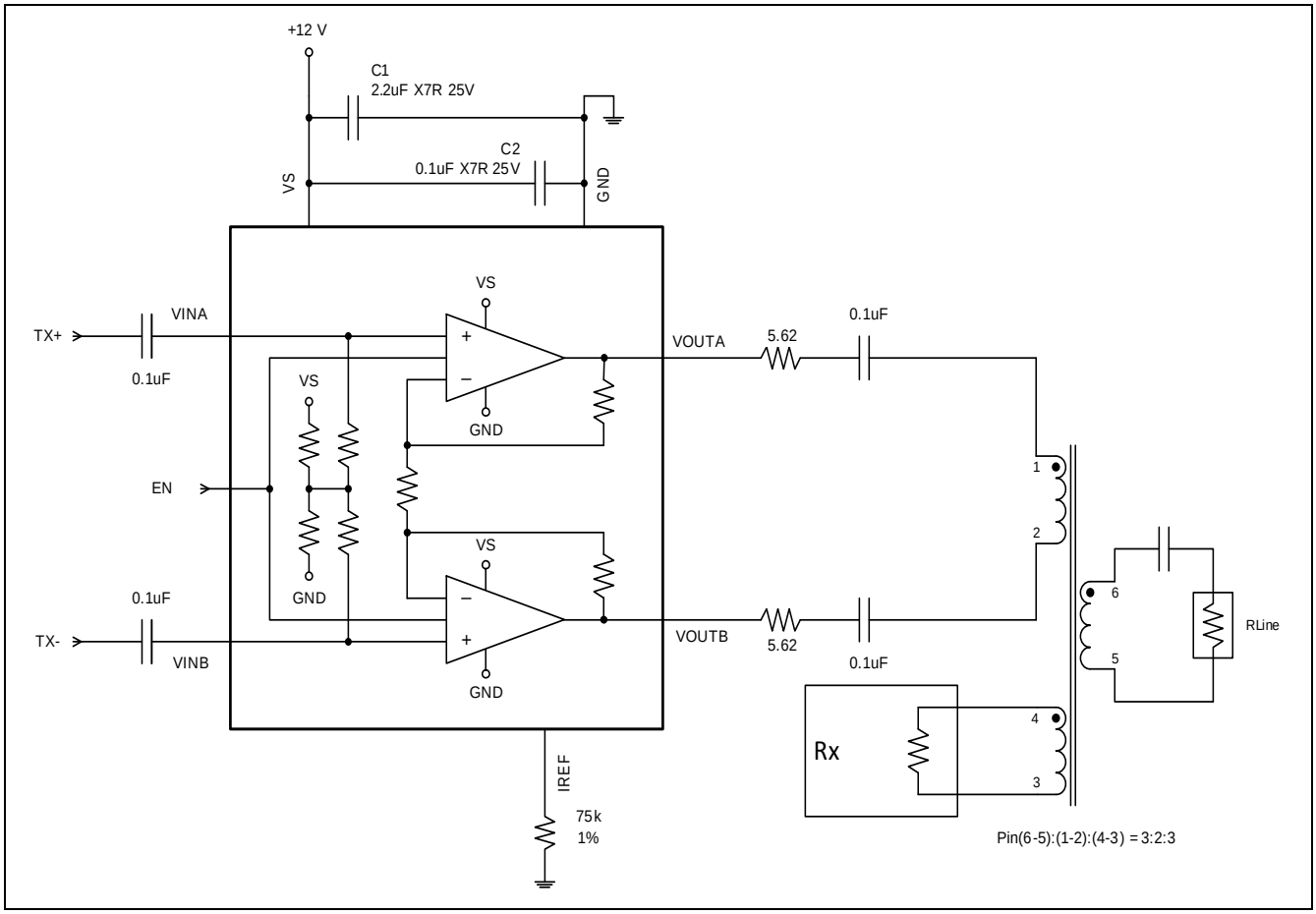


Figure 2. Typical Application Circuit - Channel 1

Input Considerations

The driving source impedance should be less than 100 nH to avoid any ringing or oscillation.

Output Driving Considerations

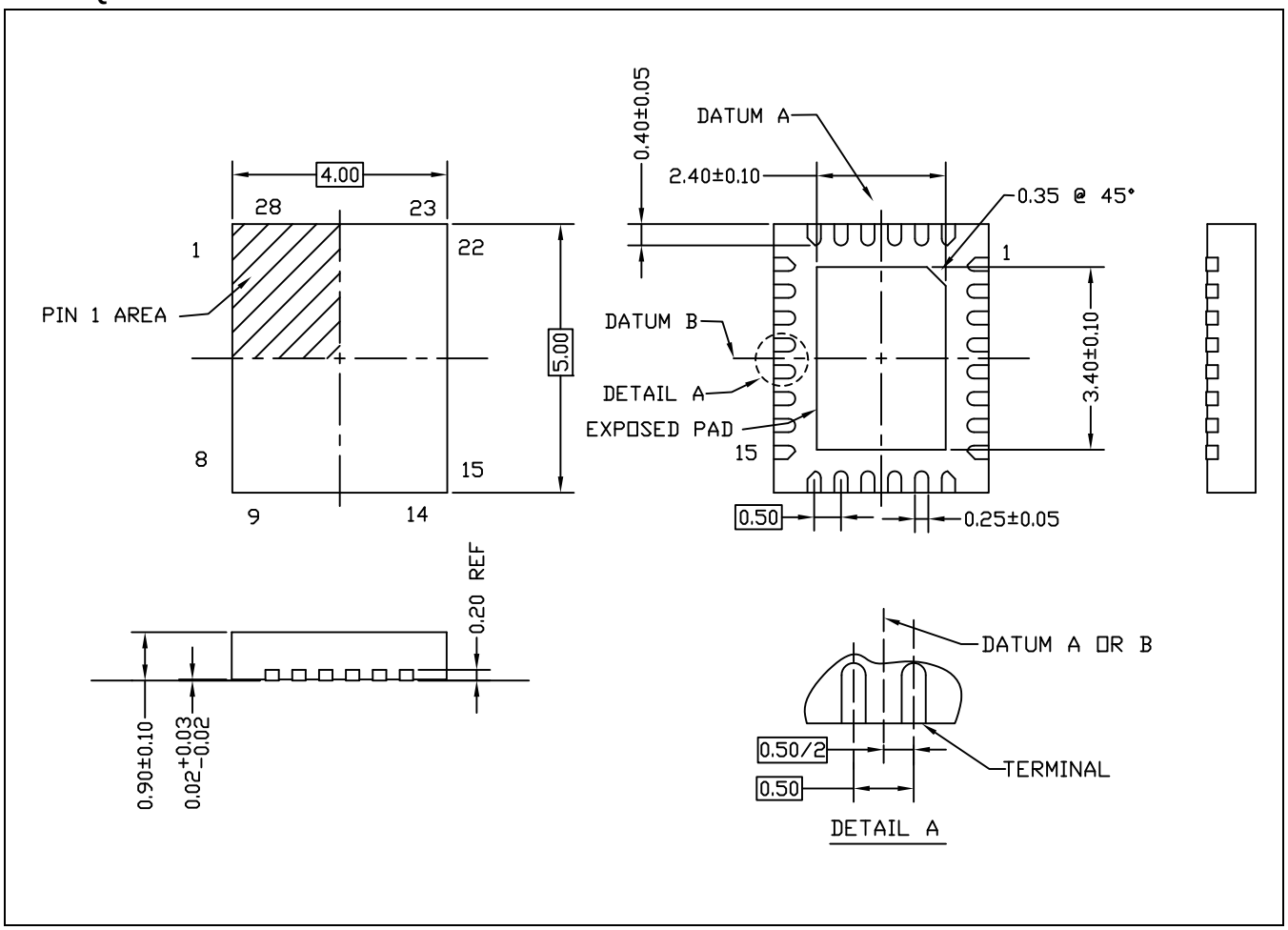
The internal metallization is designed to carry up to about 100 mA of steady DC current and there is no current limit mechanism. The device does feature integrated thermal shutdown protection however with hysteresis. Driving lines with no series resistor is not recommended.

Power Supplies and Component Placement

The power supplies should be well bypassed close to the Le87612 device. A 2.2 µF tantalum capacitor and a 0.1 µF ceramic capacitor for the VS supply is recommended.

PHYSICAL DIMENSIONS

28-Pin QFN



Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

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Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

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